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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 08/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,210	BOLES ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 12-19 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1,22,33,48 of U.S. Patent No. 6,708,268. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons (first the claims are set forth side by side for comparison below).

Patent No. 6,708,268	Instant application
1. A microcontroller comprising: a central processing unit; a data memory	12. A microcontroller comprising: a central processing unit; a data .memory.crocontroller comprising: a cent

Patent No. 6,708,268	Instant application
having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit, said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory; wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit	having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit, said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory; wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit

Patent No. 6,708,268	Instant application
indicating whether said bank select unit accesses one of said banks or said virtual bank.	Indicating whether said bank select unit accesses one of said bank orsaid virtual bank and
22. A microcontroller as in claim 1 wherein said instruction set includes an instruction with an encoding of 1110 110s kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction is a subroutine call of an entire 2 mega byte memory range, said `s` bit of said instruction is used to modify the behavior of said instruction, said memory range designated by said kkkk kkkk kkkk portions of said instruction.	wherein said instruction set includes an instruction with an encoding of 1110 110s kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction is a subroutine call of an entire 2 mega byte memory range, said `s` bit of said instruction is used to modify the behavior of said instruction, said memory range designated by said **kkkk kkkk and** kkkk kkkk kkkk portions of said instruction.
1. A microcontroller comprising: a central processing unit; a data memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an	13. A microcontroller comprising: a central processing unit; a data .memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; a

Patent No. 6,708,268	Instant application
arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit, said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory; wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank.	arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit, said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory; wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank; and
33. A microcontroller as in claim 1 wherein said instruction set includes an instruction with an encoding of 1110 1111 kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction provides an unconditional branch for a program	wherein said instruction set includes an instruction with an encoding of 1110 1111 kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction provides an unconditional branch for a program

Patent No. 6,708,268	Instant application
composed from said instruction set anywhere within a 2 megabyte memory range designated by said kkkk kkkk kkkk portions of said instruction.	composed from said instruction set anywhere within a 2 megabyte memory range designated by said kkkk kkkk and kkkk kkkk kkkk portions of said instruction.
1. A microcontroller comprising: a central processing unit; a data memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit,	14. A microcontroller comprising: a central processing unit; a data memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit,

Patent No. 6,708,268	Instant application
said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory; wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank.	said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory; wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank; and
48. A microcontroller as in claim 1 wherein said instruction set includes an instruction with an encoding of **0000 0000 0000 0000** 1111 xxxx xxxx xxxx, wherein said instruction performs no operation, and the contents of said xxxx xxxx xxxx portion of said instruction are ignored.	wherein said instruction set includes an instruction with an encoding of 1111 xxxx xxxx xxxx, wherein said instruction performs no operation, and the contents of said xxxx xxxx xxxx portion of said instruction are ignored.
1. A microcontroller comprising: a central processing unit; a data memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select	15. A microcontroller comprising: a central processing unit; a data .memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select

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unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit,	unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit,
said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory; wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank.	said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory; wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank;and

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48. A microcontroller as in claim 1 wherein said instruction set includes an instruction with an encoding of **0000 0000 0000 0000** 1111 xxxx xxxx xxxx, wherein said instruction performs no operation, and the contents of said xxxx xxxx xxxx portion of said instruction are ignored.

1. A microcontroller comprising: a central processing unit; a data memory
having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank,
whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory,
wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit,

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wherein said instruction set includes
an instruction with an encoding of 0000 0000 0000 0000,wherein said instruction performs no operation, and the contents of the latter 0000 0000 0000 portion of said instruction are ignored.

16. A microcontroller comprising: a central processing unit; a data memory
. A microcontroller comprising: a cent coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit for selecting one of said banks in said data memory,wherein said selected bank forms a register file;and an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory,
wherein one of said special function registers is a working register being coupled with said arithmetic logic unit;

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said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory; wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank.	wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank; and
22. A microcontroller as in claim 1 wherein said instruction set includes an instruction with an encoding of 1110 110s kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction is a subroutine call of an entire 2 mega byte memory range, said `s` bit of said instruction is used to modify the behavior of said instruction, said memory range designated by said kkkk kkkk kkkk portions of said instruction.	wherein said instruction set includes an instruction with an encoding of 1110 110s kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction is a subroutine call of an entire 2 mega byte memory range, said `s` bit of said instruction is used to modify the behavior of said instruction, said memory range designated by said kkkk kkkk and kkkk kkkk kkkk portions of said instruction.
1. A microcontroller comprising: a central processing unit; a data memory	17. A microcontroller comprising: a central processing unit; a data memory

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having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit,	coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit for selecting one of said banks in said data memory,wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; and a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit;
said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory;	
wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit	wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit

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indicating whether said bank select unit accesses one of said banks or said virtual bank.	indicating whether said bank select unit accesses one of said banks or said virtual bank; and
33. A microcontroller as in claim 1 wherein said instruction set includes an instruction with an encoding of 1110 1111 kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction provides an unconditional branch for a program composed from said instruction set anywhere within a 2 megabyte memory range designated by said kkkk kkkk kkkk portions of said instruction.	wherein said instruction set includes an instruction with an encoding of 1110 1111 kkkk kkkk 1111 kkkk kkkk kkkk, wherein said instruction provides an unconditional branch for a program composed from said instruction set anywhere within a 2 megabyte memory range designated by said kkkk kkkk and kkkk kkkk kkkk portions of said instruction.
1. A microcontroller comprising: a central processing unit; a data memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file;	18. . A microcontroller comprising: a central processing unit; a data .memory.crocontroller comprising: a cent coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit for selecting one of said banks in said data memory,wherein said selected bank forms a register file;and an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory,

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function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit,	wherein one of said special function registers is a working register being coupled with said arithmetic logic unit;
said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory;	
wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank.	wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank; and
48. A microcontroller as in claim 1 wherein said instruction set includes an instruction with an encoding of 0000 0000 0000 0000 1111 xxxx xxxx xxxx, wherein said instruction performs no operation, and the contents of said xxxx xxxx xxxx portion of said instruction are ignored.	wherein said instruction set includes an instruction with an encoding of 1111 xxxx xxxx xxxx, wherein said instruction performs no operation, and the contents of said xxxx xxxx xxxx portion of said instruction are ignored.

Patent No. 6,708,268	Instant appplication
1. A microcontroller comprising: a central processing unit; a data memory having a linearized address space coupled with said central processing unit being divided into n banks; said central processing unit comprising: a bank select unit which either accesses one of said banks or accesses a virtual bank, whereby said virtual bank combines partial memory space of two banks of said data memory and wherein said selected bank forms a register file; an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit; a program counter register within said central processing unit,	19. A microcontroller comprising: a central processing unit; a data memory coupled with saidrising: a cent central processing unit being divided into n banks; said central processing unit comprising: a bank select unit for selecting one of said banks in said data memory,wherein said selected bank forms a register file;and an arithmetic logic unit coupled with said register file; a plurality of special function registers being mapped to one of said banks in said data memory, wherein one of said special function registers is a working register being coupled with said arithmetic logic unit;
said program counter mapped in said data memory; and a working register within said central processing unit being coupled with said arithmetic logic unit, said working register mapped in said data memory;	

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wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank.	wherein said microcontroller having an instruction set for controlling said arithmetic logic unit and wherein at least one instruction comprises a bit indicating whether said bank select unit accesses one of said banks or said virtual bank; and
48. A microcontroller as in claim 1 wherein said instruction set includes an instruction with an encoding of 0000 0000 0000 0000 1111 xxxx xxxx xxxx, wherein said instruction performs no operation, and the contents of said xxxx xxxx xxxx portion of said instruction are ignored.	wherein said instruction set includes an instruction with an encoding of 0000 0000 0000 0000 , wherein said instruction performs no operation, and the contents of the later 0000 0000 0000 portion of said instruction are ignored.

Patent No. 6,708,268 taught the invention in the instant application substantially as claimed. The side by side showing of the claims to the Patent and the corresponding claims in the instant application above show the similarities.

As to claims 12-15 of the instant application. The portions of these claims that correspond to claim 1 are the same as in claim 1. The portion of claim 22(and 33 respectively) that is different from the claim 12(and 13 respectively) in the instant application set forth that plural portions (kkkk kkkk and kkkk kkkk kkkk) portions are used to modify the instruction. Both claims perform the same operation of using one or more encoded portions to modify the instruction of the One of ordinary skill would have been motivated utilze different portions of the instruction to modify the instruction dependent on the type of instruction at least to provided flexibility to the system in controlling the system with an instruction. This would have allowed the system to more flexibly use bits of the instruction expecially when there system used variable width or different precision instructions. As to the limitations of claims 14 and 15 the difference is that the claims 49 encodes the instruction as 0000 0000 0000 0000 1111 xxxx xxxx xxxx and ignores the xxxx xxxx xxxx portion; and the claims 14 is ignores that later (0000 0000 0000) and claim 15 ignores the xxx xxxx xxxx portions. The

claims in the application (14,15) and the claims of the patent both does the same this by performing no operation and ignoring bits of the instruction. One of ordinary skill would have been motivated to use encoding of the bits from the first portion and/or second portion of the instruction at least to provide an no-operation instruction when different width or precision instructions or compounded instructions. Where the use of a no-operation instruction would at least have been necessary to adjust in the timing between processing of instructions. Claims 16,17,18,19 in the instant application contain elements perform operations that are in claim 1 of claim the patent as shown with the side to side listing of the claims above. The features that are not specifically shown in claim 1 of the patent are obvious for the same reasons as the claims 12-15 (for claims 16-19 respectively of the instant application) discussed above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patrick (patent No. 5,734,858) disclosed a system for simulating banked memory as a linear address space (e.g., see abstract).

Dockser (patent No. 5,613,151) disclosed a system with flexible register mapping scheme (e.g., see abstract).

Lau (patent No. 5,553,023) disclosed a system with memory partitioning (e.g., see abstract).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER